The blind, anonymous survey was emailed to thousands of SoC and IC design professionals worldwide by an independent firm in Q1 2013. A total of 372 engineering professionals responded, with approximately half in management roles.

Given time to market pressures, engineering groups are toward ‘continuous design’. These overlapping design starts are driving IP-based design and IP reuse methodologies. This report focuses closely on IP reuse for design and verification across the enterprise, including both digital and custom/analog design.

This is the fifth annual survey report related to Design and IP Management. The topics covered are:

I. Survey methodology and demographics
II. Non-Memory SoC & IC design composition: Internal IP, 3rd party IP, new content
III. IP Reuse and Verification
   a. Key verification tasks, inefficiencies
   b. Checklist for managing IP verification
IV. Top IP reuse dependency management challenges
V. Percentage of tape outs with known bugs
VI. Measured ROI from IP reuse dependency management system
VII. Organizational incentives to increase internal IP reuse.
VIII. Summary

I. Survey Methodology and Demographics

A blind, anonymous survey was emailed to several thousand SoC/IC design professionals worldwide by an independent firm during January and February of 2013. 372 engineers and managers completed the survey online. The survey respondents included of a broad spectrum of designers and engineering management.

Approximately half of respondents held positions in engineering, verification, project or CAD management. 28 percent were designers (digital 18%, custom-analog 6%, and FPGA 4%) and 11% were verification engineers.
II. Non-Memory SoC & IC Design composition: Internal IP, 3\textsuperscript{rd} party IP, new content

One finding of this year’s survey underscored the prevalence of IP reuse. In 2013, respondents expect an average of:

- 68 percent of their non-memory SoC and IC design content to be reused IP
- 32 percent to be new design content
- Almost two-thirds of their reused IP to be internal IP, with the remainder third party IP

An IP-based approach is still commonly used for the new design content created. The design is partitioned into 'IP modules' which are then developed in parallel with the rest of the design.
III. IP Reuse and Verification

--Key verification tasks, inefficiencies--

Both design reuse and verification reuse must be addressed to truly achieve IP reuse efficiencies. The chart below shows where verification teams spend their time. This information helps to more measurably determine the potential time and resource reductions that could be achieved with effective dependency management and reuse.

Verification time is primarily spent as follows:

- Developing testbenches (26%)
- Writing and running the tests (26%)
- Debugging (42%). Debugging time can be broken down into:
  - Identifying bugs (25%)
  - Managing the bug dependencies, including tracing instances/history, bug notification, and propagating fixes (17%)

Thus verification engineers spend an average of 60% of their debugging time on identifying bugs, and 40% on managing bug dependencies.

Each verification task has inefficiencies that can be addressed with effective IP reuse.

- Testbench development time - can be reduced by tying the IP testbench with the IP. This eliminates redundancies in creating testbenches; it also avoids the overhead in tracking them down and the need to find the proper IP testbench version because it is not tied to the proper IP version.
- Time spent writing and running tests - can be cut down by ensuring that all verification information associated with an IP - including whether or not it works under certain conditions, plus any assertions - is encapsulated with the IP.

- Debugging Time. If a bug is found in an IP, designers using other instances of the IP need to be properly notified to reduce redundancies from multiple teams debugging the same problem in multiple instances of an IP. Further, minimizing the overhead associated with identifying and managing bug dependencies is a clear opportunity to reduce debug time.

--Checklist for managing IP verification--

Survey participants were asked to identify the IP module verification checklist items that would be useful for their organization to track for engineering and management access/viewing. Each participant selected an average of 6 items they would like to track, with a lot of variability after the first few items. The rankings are below. This question focused on digital verification; however multiple respondents noted that they also wanted to track a custom/analog verification checklist.

<table>
<thead>
<tr>
<th>IP Verification Checklist Items Desired to be Tracked</th>
<th>Percentage</th>
</tr>
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<tbody>
<tr>
<td>RTL regression</td>
<td>71%</td>
</tr>
<tr>
<td>Functional/ assertion/ test coverage</td>
<td>63%</td>
</tr>
<tr>
<td>Clock domain crossing verified</td>
<td>58%</td>
</tr>
<tr>
<td>Gate-level regression</td>
<td>50%</td>
</tr>
<tr>
<td>DFT /Scan /BIST simulation at specified corners</td>
<td>50%</td>
</tr>
<tr>
<td>Formal model/protocol checks</td>
<td>50%</td>
</tr>
<tr>
<td>Post-scan insertion logic equivalence checking</td>
<td>45%</td>
</tr>
<tr>
<td>Pin list &amp; specification match</td>
<td>44%</td>
</tr>
<tr>
<td>Pre-scan logic equivalence checking</td>
<td>41%</td>
</tr>
<tr>
<td>Line code coverage</td>
<td>39%</td>
</tr>
<tr>
<td>State &amp; transition code coverage</td>
<td>33%</td>
</tr>
<tr>
<td>Condition code coverage</td>
<td>32%</td>
</tr>
<tr>
<td>Expression code coverage</td>
<td>29%</td>
</tr>
<tr>
<td>Don't know</td>
<td>10%</td>
</tr>
<tr>
<td>Other</td>
<td>3%</td>
</tr>
</tbody>
</table>
IV. Top IP Reuse Dependency Management Challenges

IP reuse dependency management spans chip designers, IP owners, verification engineers, project leads, design and verification managers and CAD managers. They all need ready access to the information regarding the IP being reused. We asked all these team members to rank their top 3 challenges with the management of the interdependencies associated with IP reuse. Below are their rankings.

<table>
<thead>
<tr>
<th>IP Reuse Dependency Management Top Challenges</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Managing multiple data sources</td>
<td>43%</td>
</tr>
<tr>
<td>Testbenches for IP not adequately shared/reused</td>
<td>42%</td>
</tr>
<tr>
<td>IP Development or verification steps not enforced/tracked</td>
<td>40%</td>
</tr>
<tr>
<td>Unknown IP usage, notifying IP users re known bugs/fixes</td>
<td>40%</td>
</tr>
<tr>
<td>3rd party IP provider &amp; internal team data exchange</td>
<td>37%</td>
</tr>
<tr>
<td>Lack of processes and/or designer participation</td>
<td>35%</td>
</tr>
<tr>
<td>Key IP properties/status items not tied to IP</td>
<td>19%</td>
</tr>
<tr>
<td>Bug roll-up reporting</td>
<td>16%</td>
</tr>
<tr>
<td>Other</td>
<td>8%</td>
</tr>
</tbody>
</table>

1. Managing multiple data sources (43%). The top challenge cited was managing the mix of data sources. Organizations must manage IP from different systems, both from 3rd parties as well as inside the company. Companies will often have a combination of commercial design management systems, open source revision control, and internally developed systems, all used by different groups. The digital groups often use a different system than the custom/analog groups, which can make sharing information difficult.

2. Testbenches for IP modules not adequately shared/reused (42%). Organizations recognize the redundancies in testbench development, which could be addressed via improved reuse.

3. Unknown IP usage vs. product releases & difficulty notifying IP user re known bugs/fixes (40%). One complex issue for dependency management is tracing an IP bug backwards and forwards in the history to identify all IP instances across designs and derivatives. Additionally, timely notification of the bug and fixes is required.

4. IP development or verification steps not enforced/tracked (40%). One of the challenges of reusing IP is that the IP development and verification processes are not set up for reuse. This kind of checklist is not intended to be a gating item for using the IP, but rather to provide a discipline to communicate ongoing status. It gives the designers greater confidence when using an IP.
5. 3rd party IP provider & internal teams data exchange (37%). Teams count on robust 3rd party IP, but this also has multiple versions over time, and those dependencies must also be managed.

6. Lack of processes and/or designer participation (35%). Without the organizational infrastructure, incentives and discipline, companies don’t get the consistent participation needed for efficient IP reuse.

7. Key IP properties/status items not tied to IP (19%). IP reuse is clearly problematic if required information beyond the design code is missing or not easily found in the IP database.

8. Bug roll-up reporting (16%). Management, chip project leads and the IP owners want to see the bugs associated with all instances of a particular IP or a specific design.

V. Percentage of tape outs with known bugs

To measure one aspect of the complexities of dependency management, respondents were asked if they had ever taped out with a known bug. An example of this would be correcting a bug in one instance of an IP, but missing the same bug in another IP instance.

Of the engineering, verification, project and CAD managers that knew this answer, a whopping 44% percent answered that yes their organizations had taped out a design with a known bug due to dependency management failures.

The average delay cited by all respondents for taping out with a known bug was six weeks. This average delay includes those able to avoid any delay by finding a work around for the bug.
VI. Measured Results from Implementing IP Reuse Dependency Management Systems

Let’s look at what this year’s survey respondents cited as the results they achieved from implementing IP reuse dependency management processes and systems.

Companies that instituted significant IP reuse dependency management processes/systems and shared their results achieved an average:

- 31% reduction in engineering resources, and
- 30% faster time to market

These results show substantial improvements.
VII. Organizational Incentives for Increasing & Improving internal IP reuse

62 percent of respondents stated their organization had incentives to increase/improve reuse of internal design IP.

56 percent said their organization had incentives to improve reuse of internal verification IP.

Many respondents offered feedback as to which incentives worked best to encouraging and improve IP reuse.

- The incentive cited most often was the resource reduction and the shortened time to market from having an effective process and technology system in place.

- Multiple respondents said that formal planning and processes were a strong incentive.

- Other incentives included clear ownership, encouragement to participate, and having a culture valuing IP reuse.

Some respondents cited obstacles to avoid in gaining team commitment to IP reuse. They commented that management understanding and commitment was a critical element, with an upfront IP roadmap and planning.

They noted that insufficient methodology guidelines and rules can make reuse difficult or impossible, yet reuse design guidelines on their own were inadequate without the corresponding infrastructure. Multiple people commented that an obstacle to success was the lack of a proper technology infrastructure to facilitate IP reuse.

VIII. Summary

IP-based design is a dominant methodology today, encompassing new design as well as internal and third party IP reuse. The specific goal of IP reuse is that designers find the IP they need, plug it in, and it works. To ensure that IP reuse takes less time than creating and verifying new content, it must address both the design and the verification elements. This creates a complex dependency management and
communication requirement, spanning designers, verification teams, project leads, and CAD and engineering management.

Effective IP reuse requires both a technology infrastructure and clear management processes. An easy to deploy IP reuse dependency management system, with appropriate top-down direction and incentives, will motivate team members to participate. Finally, the top incentive for team member participation is to directly experiencing the efficiency and time to market advantages from their first effort.

A major goal of IP reuse dependency management is to have a higher return on assets. Users found improvements of approximately 30 percent in both resource reductions and improved time to market.

About IC Manage

IC Manage provides high performance design data and IP management solutions for companies to efficiently collaborate on single and multi-site designs. IC Manage lets designers dynamically track, control and distribute library, block-level and SOC design data, including configurations and properties. Design teams can improve product quality, designer productivity, team collaboration, bug dependency tracking, plus maximize IP reuse. IC Manage is headquartered at 2105 South Bascom Ave., Suite 120, Campbell, CA. For more information visit us at www.icmanage.com.

Shiv Sikand, Vice President of Engineering, IC Manage

Shiv founded IC Manage in 2003, and has been instrumental in the company achieving technology leadership in high performance design and IP management solutions. Prior to IC Manage, Shiv was at Matrix Semiconductor, where he worked on the world's first 3D memory chips.

Shiv also worked at MIPS, where he led the development of the MIPS Circuit Checker (MCC). While working on the MIPS processor families at SGI, Shiv created and deployed cdsp4, the Cadence-Perforce integration, which he later open sourced. Cdsp4 provided the inspiration and architectural testing ground for IC Manage. Shiv received his BSc and MSc degrees in Physics and Electrical Engineering from the University of Manchester Institute of Science and Technology.

Other references:

Global Design Management Report 2012
Dean Drako on IP Reuse 2.0 -- Design AND Verification